Based on 64Mx16 (1GB) / 128Mx8 (2GB) DDR3 SDRAM A-Die

Features

•Performance:

Speed Sort	PC3-8500	PC3-10660	Unit
	-BE	-CG	
DIMM CAS Latency	7	9	
fck – Clock Freqency	533	667	MHz
tck – Clock Cycle	1.875	1.5	ns
fDQ – DQ Burst Freqency	1066	1333	Mbps

- 204-Pin Small Outline Dual In-Line Memory Module (SO-DIMM)
- 1GB: 128Mx64 Unbuffered DDR3 SO-DIMM based on 64Mx16 DDR3 SDRAM A-Die devices.
- 2GB: 256Mx64 Unbuffered DDR3 SO-DIMM based on 128Mx8 DDR3 SDRAM A-Die devices.
- Intended for 533MHz/667MHz/800MHz applications
- Inputs and outputs are SSTL-15 compatible
- $V_{DD} = V_{DDQ} = 1.5V \pm 0.075V$
- SDRAMs have 8 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- DRAM DLL aligns DQ and DQS transitions with clock transitions.
- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
  - DIMM $\overline{CAS}$ Latency: 5,6,7,8,9,10
  - Burst Type: Sequential or Interleave
  - Burst Length: BC4, BL8
  - Operation: Burst Read and Write
- Two different termination values (Rtt_Nom & Rtt_WR)
- 13/10/2 (row/column/rank) Addressing for 1GB
- 14/10/2 (row/column/rank) Addressing for 2GB
- Extended operating temperature rage
- Auto Self-Refresh option
- Serial Presence Detect
- Gold contacts
- 1GB: SDRAMs are in 96-ball BGA Package
- 2GB: SDRAMs are in 78-ball BGA Package
- RoHS compliance

Description

M2N1G64CBH8A5P and M2N2G64CB8HA5N are unbuffered 204-Pin Double Data Rate 3 (DDR3) Synchronous DRAM Small Outline Dual In-Line Memory Module (SO-DIMM), organized as two ranks of 128Mx64 (1GB) and 256Mx64 (2GB) high-speed memory array. Modules use eight 64Mx16 (1GB) 96-ball BGA packaged devices and sixteen 128Mx8 (2GB) 78-ball BGA packaged devices. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All Elixir DDR3 SODIMMs provide a high-performance, flexible 8-byte interface in a space-saving footprint.

The DIMM is intended for use in applications operating of 533MHz/667MHz/800MHz clock speeds and achieves high-speed data transfer rates of 1066Mbps/1333Mbps/1600Mbps. Prior to any access operation, the device $\overline{CAS}$ latency and burst/length/operation type must be programmed into the DIMM by address inputs A0-A12 (1GB)/A0-A13 (2GB) and I/O inputs BA0~BA2 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial EEPROM using a standard IIC protocol. The first 128 bytes of SPD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

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Ordering Information

Part Number	Speed			Organization	Power	Leads	Note
M2N1G64CBH8A5P-BE	DDR3-1066	PC3-8500	533MHz (1.875ns @ CL = 7)	128Mx64	1.5V	Gold	
M2N1G64CBH8A5P-CG	DDR3-1333	PC3-10600	667MHz (1.500ns @ CL = 9)				
M2N2G64CB8HA5N-BE	DDR3-1066	PC3-8500	533MHz (1.875ns @ CL = 7)	256Mx64			
M2N2G64CB8HA5N-CG	DDR3-1333	PC3-10600	667MHz (1.500ns @ CL = 9)				

Pin Description

CK0, CK1	Clock Inputs, positive line	DQ0-DQ63	Data input/output
$\overline{CK0}$, $\overline{CK1}$	Clock Inputs, negative line	DQS0-DQS7	Data strobes
CKE0, CKE1	Clock Enable	$\overline{DQS0}$-$\overline{DQS7}$	Data strobes complement
$\overline{RAS}$	Row Address Strobe	DM0-DM7	Data Masks
$\overline{CAS}$	Column Address Strobe	$\overline{EVENT}$	Temperature event pin
$\overline{WE}$	Write Enable	$\overline{RESET}$	Reset pin
$\overline{S0}$, $\overline{S1}$	Chip Selects	V_{REFDQ} , V_{REFCA}	Input/Output Reference
A0-A9, A11, A13	Address Inputs	V_{DDSPD}	SPD and Temp sensor power
A10/AP	Address Input/Auto-Precharge	SA0, SA1	Serial Presence Detect Address Inputs
A12/$\overline{BC}$	Address Input/Burst Chop	Vtt	Termination voltage
BA0-BA2	SDRAM Bank Address Inputs	V_{SS}	Ground
ODT0, ODT1	Active termination control lines	V_{DD}	Core and I/O power
SCL	Serial Presence Detect Clock Input	NC	No Connect
SDA	Serial Presence Detect Data input/output		
Note: A13 is only support in 2GB module type.			

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1GB/2GB DDR3 SDRAM SODIMM Pinout

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REFDQ}	2	V_{SS}	53	DQ19	54	V_{SS}	105	V_{DD}	106	V_{DD}	155	V_{SS}	156	V_{SS}
3	V_{SS}	4	DQ4	55	V_{SS}	56	DQ28	107	A10/AP	108	BA1	157	DQ42	158	DQ46
5	DQ0	6	DQ5	57	DQ24	58	DQ29	109	BA0	110	$\overline{RAS}$	159	DQ43	160	DQ47
7	DQ1	8	V_{SS}	59	DQ25	60	V_{SS}	111	V_{DD}	112	V_{DD}	161	V_{SS}	162	V_{SS}
9	V_{SS}	10	$\overline{DQS0}$	61	V_{SS}	62	$\overline{DQS3}$	113	$\overline{WE}$	114	$\overline{S0}$	163	DQ48	164	DQ52
11	DM0	12	DQS0	63	DM3	64	DQS3	115	$\overline{CAS}$	116	ODT0	165	DQ49	166	DQ53
13	V_{SS}	14	V_{SS}	65	V_{SS}	66	V_{SS}	117	V_{DD}	118	V_{DD}	167	V_{SS}	168	V_{SS}
15	DQ2	16	DQ6	67	DQ26	68	DQ30	119	A13/NC	120	ODT1	169	$\overline{DQS6}$	170	DM6
17	DQ3	18	DQ7	69	DQ27	70	DQ31	121	$\overline{S1}$	122	NC	171	DQS6	172	V_{SS}
19	V_{SS}	20	V_{SS}	71	V_{SS}	72	V_{SS}	123	V_{DD}	124	V_{DD}	173	V_{SS}	174	DQ54
21	DQ8	22	DQ12	73	CKE0	74	CKE1	125	NC	126	V_{REFCA}	175	DQ50	176	DQ55
23	DQ9	24	DQ13	75	V_{DD}	76	V_{DD}	127	V_{SS}	128	V_{SS}	177	DQ51	178	V_{SS}
25	V_{SS}	26	V_{SS}	77	NC	78	NC	129	DQ32	130	DQ36	179	V_{SS}	180	DQ60
27	$\overline{DQS1}$	28	DM1	79	BA2	80	NC	131	DQ33	132	DQ37	181	DQ56	182	DQ61
29	DQS1	30	$\overline{RESET}$	81	V_{DD}	82	V_{DD}	133	V_{SS}	134	V_{SS}	183	DQ57	184	V_{SS}
31	V_{SS}	32	V_{SS}	83	A12/$\overline{BC}$	84	A11	135	$\overline{DQS4}$	136	DM4	185	V_{SS}	186	$\overline{DQS7}$
33	DQ10	34	DQ14	85	A9	86	A7	137	DQS4	138	V_{SS}	187	DM7	188	DQS7
35	DQ11	36	DQ15	87	V_{DD}	88	V_{DD}	139	V_{SS}	140	DQ38	189	V_{SS}	190	V_{SS}
37	V_{SS}	38	V_{SS}	89	A8	90	A6	141	DQ34	142	DQ39	191	DQ58	192	DQ62
39	DQ16	40	DQ20	91	A5	92	A4	143	DQ35	144	V_{SS}	193	DQ59	194	DQ63
41	DQ17	42	DQ21	93	V_{DD}	94	V_{DD}	145	V_{SS}	146	DQ44	195	V_{SS}	196	V_{SS}
43	V_{SS}	44	V_{SS}	95	A3	96	A2	147	DQ40	148	DQ45	197	SA0	198	$\overline{EVENT}$
45	$\overline{DQS2}$	46	DM2	97	A1	98	A0	149	DQ41	150	V_{SS}	199	V_{DDSPD}	200	SDA
47	DQS2	48	V_{SS}	99	V_{DD}	100	V_{DD}	151	V_{SS}	152	$\overline{DQS5}$	201	SA1	202	SCL
49	V_{SS}	50	DQ22	101	CK0	102	CK1	153	DM5	154	DQS5	203	Vtt	204	Vtt
51	DQ18	52	DQ23	103	$\overline{CK0}$	104	$\overline{CK1}$								

Note: A13 is for 2GB modules only.

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Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0, CK1 $\overline{CK0}$, $\overline{CK1}$	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0, CKE1	Input	Active High	Activates the DDR3 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S0}$, $\overline{S1}$	Input	Active Low	Enables the associated DDR3 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue, Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the positive rising edge of CK and falling edge of $\overline{CK}$, signals $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
ODT0, ODT1	Input	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR3 SDRAM mode register.
DM0 – DM7	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS0 – DQS7 $\overline{DQS0}$ – $\overline{DQS7}$	I/O	Cross point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR3 SDRAM and is sent at the leading edge of the data window. $\overline{DQS}$ Signals are complements, and timing is relative to the cross point of respective DQS and $\overline{DQS}$. If the module is to be operated in single ended strobe mode, all $\overline{DQS}$ signals must be tied on the system board to V_{SS} and DDR3 SDRAM mode registers programmed appropriately.
BA0, BA1, BA2	Input	-	Selects which DDR3 SDRAM internal bank of four or eight is activated.
A0 – A9 A10/AP A11 A12/$\overline{BC}$ A13	Input	-	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
DQ0 – DQ63	Input	-	Data Input/Output pins.
V_{DD}, V_{DDSPD}, V_{SS}	Supply	-	Power supplies for core, I/O, Serial Presence Detect, Temp sensor, and ground for the module.
V_{REFDQ}, V_{REFCA}	Supply	-	Reference voltage for SSTL15 inputs
SDA	I/O	-	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM and temp sensor. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pull up.
SCL	Input	-	This signal is used to clock data into and out of the SPD EEPROM and Temp sensor.
SA0 – SA2	Input	-	Address pins used to select the Serial Presence Detect and Temp sensor base address.
$\overline{EVENT}$	Output	-	The $\overline{EVENT}$ pin is reserved for use to flag critical module temperature.
$\overline{RESET}$	Input	-	This signal resets the DDR3 SDRAM

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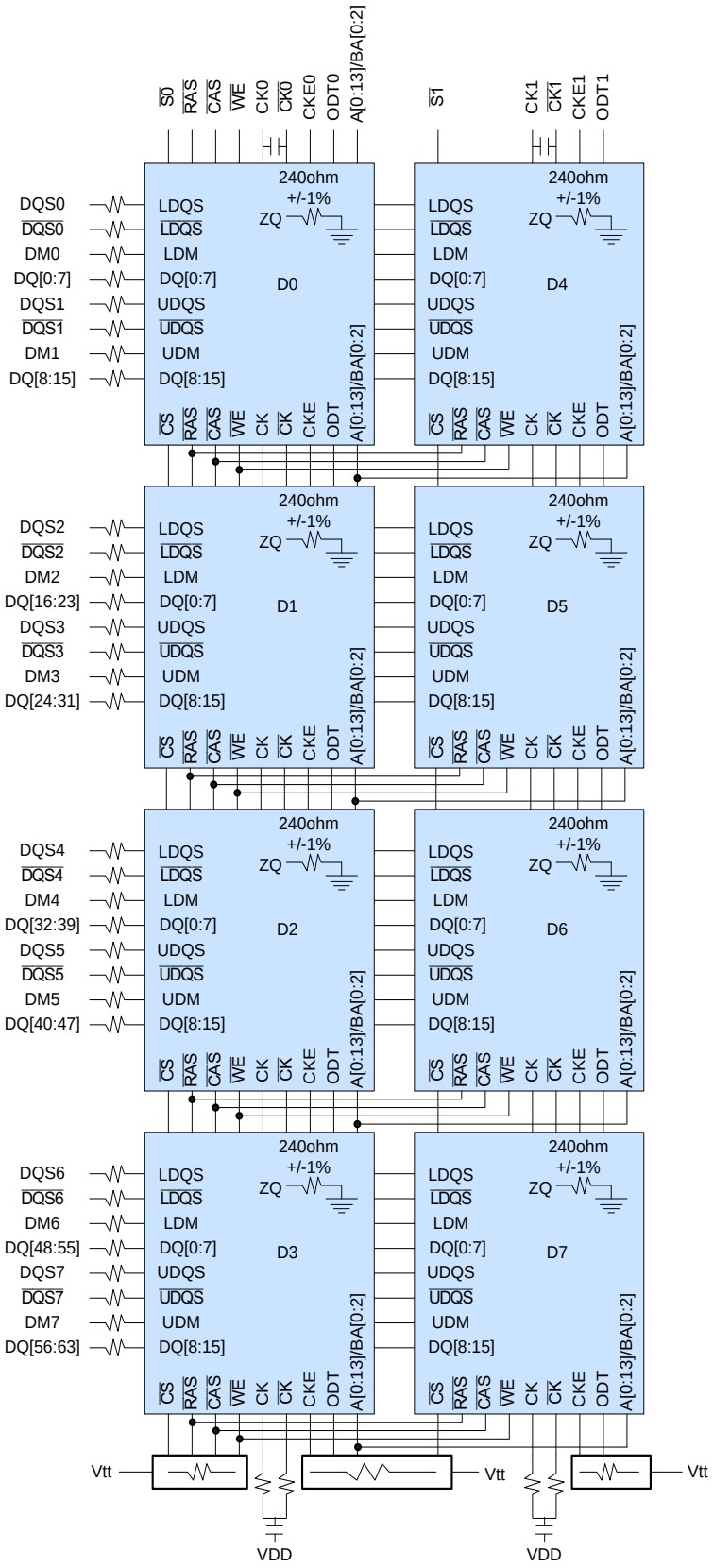
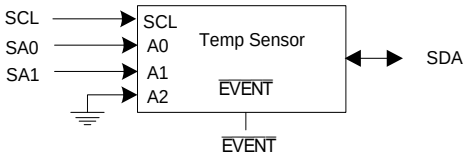
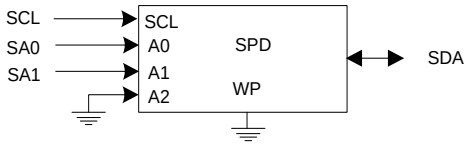
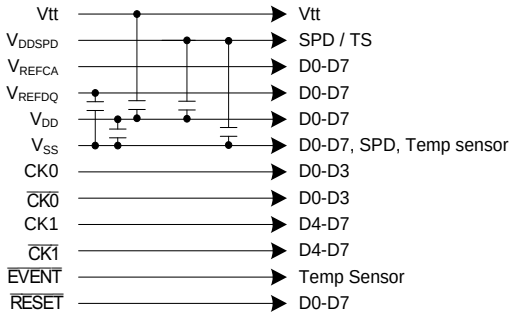
Functional Block Diagram

[1GB – 2 Ranks, 64Mx16 DDR3 SDRAMs]









Notes :

1. DQ wiring may differ from that shown however, DQ, DM, DQS, and $\overline{DQS}$ relationships are maintained as shown.

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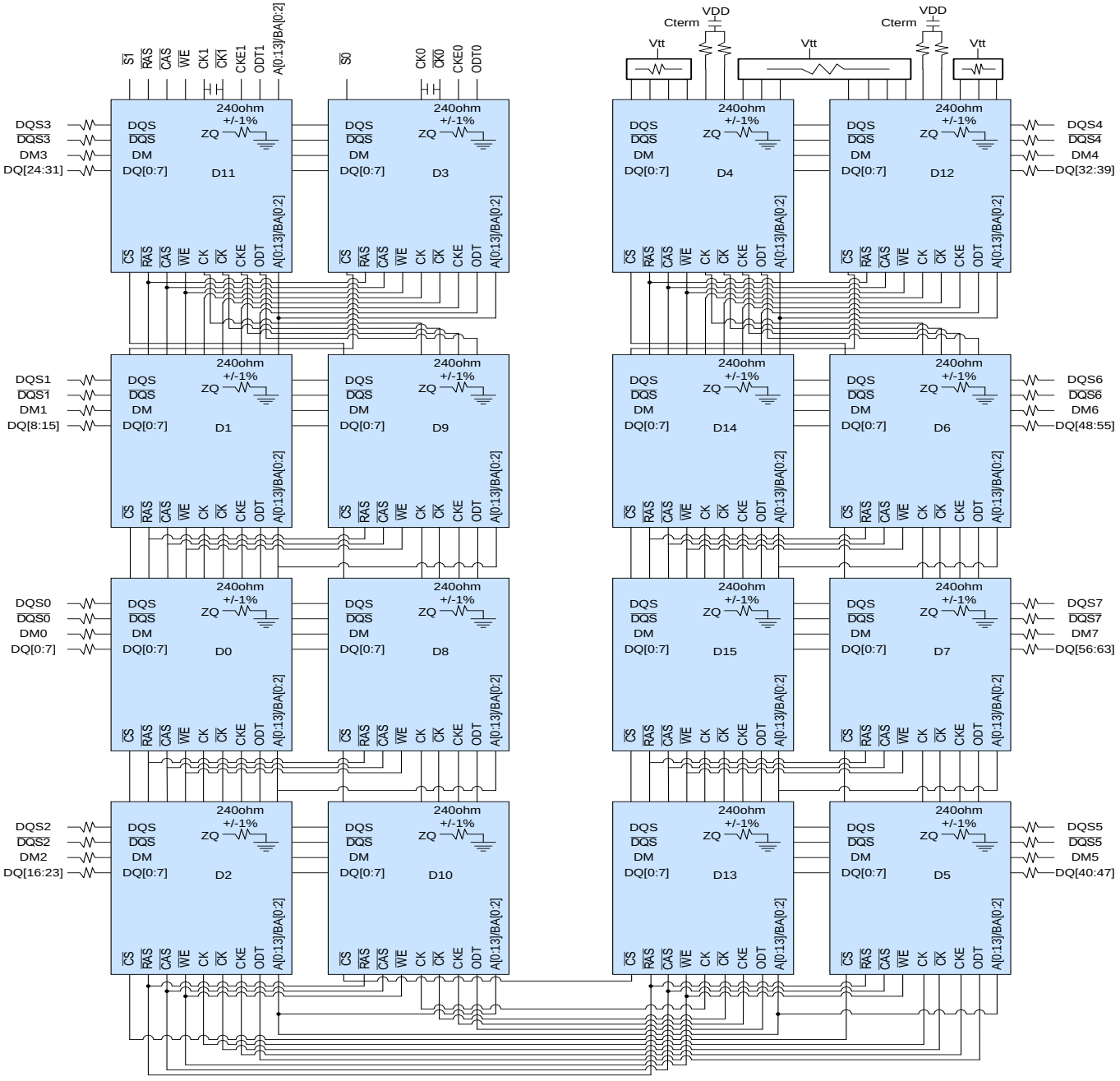
Functional Block Diagram

[2GB – 2 Ranks, 128Mx8 DDR3 SDRAMs]



Notes :

1. DQ wiring may differ from that shown however, DQ, DM, DQS, and $\overline{DQS}$ relationships are maintained as shown.

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Serial Presence Detect -- Part 1 of 2 (1GB)

128Mx64 2Ranks DDR3 SODIMM based on 64Mx16, 1.5V DDR3 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		-BE	-CG	-BE	-CG	
0	CRC range, EEPROM bytes, bytes used	CRC Covers Bytes: 0~116, Total SPD Bytes: 256, SPD Bytes Used: 176,		92		
1	SPD revision	Revision 10		10		
2	DRAM device type	DDR3 SDRAM		0B		
3	Module type (form factor)	SO-DIMM		03		
4	SDRAM Device density and banks	8 banks, 1Gb		02		
5	SDRAM device row and column count	13 rows, 10 columns		09		
6	Reserved	Undefined		00		
7	Module ranks and device DQ count	2 ranks, 16 bits		0A		
8	ECC tag and module memory Bus width	Non ECC, 64bits		03		
9	Fine timebase dividend/divisor (in ps)	2.5ps		52		
10	Medium timebase dividend	1ns		01		
11	Medium timebase divisor	8ns		08		
12	Minimum SDRAM cycle time (tCKmin)	1.875ns	1.5ns	0F	0C	
13	Reserved	Undefined		00		
14	CAS latencies supported	6,7,8	6,8,9	1C	34	
15	CAS latencies supported	Undefined		00		
16	Minimum CAS latency time (tAAmin)	13.125ns	13.5ns	69	6C	
17	Minimum write recovery time (tWRmin)	15ns		78		
18	Minimum CAS-to-CAS delay (tRCDmin)	13.125ns	13.5ns	69	6C	
19	Minimum Row Active to Row Active delay (tRRDmin)	10ns	7.5ns	50	3C	
20	Minimum row Precharge delay (tRPmin)	13.125ns	13.5ns	69	6C	
21	Upper nibble for tRAS and tRC	1,1		11		
22	Minimum Active-to-Precharge delay (tRASmin)	37.5ns	36ns	2C	20	
23	Minimum Active-to-Active/Refresh delay (tRCmin)	50.625ns	49.5ns	95	8C	
24	Minimum refresh recovery delay (tRFCmin) LSB	(Combo bytes 24,25)		70		
25	Minimum refresh recovery delay (tRFCmin) MSB	110ns		03		
26	Minimum internal Write-to-Read command delay (tWTRmin)	7.5ns		3C		
27	Minimum internal Read-to-Precharge command delay (tRTPmin)	7.5ns		3C		
28	Minimum four active window delay (tFAWmin) LSB	(Combo byte 28, 29)		01		
29	Minimum four active window delay (tFAWmin) MSB	50ns	45ns	90	68	
30	SDRAM device output drivers suported	RZQ / 6, RZQ / 7, DLL-Off Mode Support,		83		
31	SDRAM device thermal and refresh options	Extended Temperature Range, ASR, ODTS, PASR,		8D		
32	Module thermal sensor	Non Thermal Sensor Support		00		
33	SDRAM device type	Standard Monolithic Device		00		
34-59	Reserved	Undefined		--		
60	Module height (nominal)	29 < height ≦ 30 mm		0F		

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Serial Presence Detect -- Part 2 of 2 (1GB)

128Mx64 2Ranks DDR3 SODIMM based on 64Mx16, 1.5V DDR3 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		-BE	-CG	-BE	-CG	
61	Module thickness (Max)	Back: 1 < thickness ≤ 2 mm, Front: 1 < thickness ≤ 2 mm,		11		
62	Raw Card ID reference	Raw Card A		00		
63	DRAM address mapping edge connector	Undefined		00		
64-116	Reserved			--		
117-118	Module manufacture ID			830B		
119-125	Module information			--		
126-127	CRC			5309	BD5F	
128-145	Module part number	Undefined		--		
146	Module die revision	Undefined		00		
147	Module PCB revision	Nanya Technology		00		
148-149	DRAM device manufacturer ID			830B		
150-175	Manufacturer reserved	Undefined		--		
176-255	Customer reserved			--		

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Serial Presence Detect -- Part 1 of 2 (2GB)

256Mx64 2Ranks DDR3 SODIMM based on 128Mx8, 1.5V DDR3 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		-BE	-CG	-BE	-CG	
0	CRC range, EEPROM bytes, bytes used	CRC Covers Bytes: 0~116, Total SPD Bytes: 256, SPD Bytes Used: 176,		92		
1	SPD revision	Revision 10		10		
2	DRAM device type	DDR3 SDRAM		0B		
3	Module type (form factor)	SO-DIMM		03		
4	SDRAM Device density and banks	8 banks, 1Gb		02		
5	SDRAM device row and column count	14 rows, 10 columns		11		
6	Reserved	Undefined		00		
7	Module ranks and device DQ count	2 ranks, 8 bits		09		
8	ECC tag and module memory Bus width	Non ECC, 64bits		03		
9	Fine timebase dividend/divisor (in ps)	2.5ps		52		
10	Medium timebase dividend	1ns		01		
11	Medium timebase divisor	8ns		08		
12	Minimum SDRAM cycle time (tCKmin)	1.875ns	1.5ns	0F	0C	
13	Reserved	Undefined		00		
14	CAS latencies supported	6,7,8	6,8,9	1C	34	
15	CAS latencies supported	Undefined		00		
16	Minimum CAS latency time (tAAmin)	13.125ns	13.5ns	69	6C	
17	Minimum write recovery time (tWRmin)	15ns		78		
18	Minimum CAS-to-CAS delay (tRCDmin)	13.125ns	13.5ns	69	6C	
19	Minimum Row Active to Row Active delay (tRRDmin)	7.5ns	6ns	3C	30	
20	Minimum row Precharge delay (tRPmin)	13.125ns	13.5ns	69	6C	
21	Upper nibble for tRAS and tRC	1,1		11		
22	Minimum Active-to-Precharge delay (tRASmin)	37.5ns	36ns	2C	20	
23	Minimum Active-to-Active/Refresh delay (tRCmin)	50.625ns	49.5ns	95	8C	
24	Minimum refresh recovery delay (tRFCmin) LSB	(Combo bytes 24,25)		70		
25	Minimum refresh recovery delay (tRFCmin) MSB	110ns		03		
26	Minimum internal Write-to-Read command delay (tWTRmin)	7.5ns		3C		
27	Minimum internal Read-to-Precharge command delay (tRTPmin)	7.5ns		3C		
28	Minimum four active window delay (tFAWmin) LSB	(Combo byte 28, 29)		01	00	
29	Minimum four active window delay (tFAWmin) MSB	37.5ns	30ns	2C	F0	
30	SDRAM device output drivers suported	RZQ / 6, RZQ / 7, DLL-Off Mode Support,		83		
31	SDRAM device thermal and refresh options	Extended Temperature Range, ASR, ODTS, PASR,		8D		
32	Module thermal sensor	Non Thermal Sensor Support		00		
33	SDRAM device type	Standard Monolithic Device		00		
34-59	Reserved	Undefined		--		
60	Module height (nominal)	29 < height ≦ 30 mm		0F		

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Serial Presence Detect -- Part 2 of 2 (1GB)

256Mx64 2Ranks DDR3 SODIMM based on 128Mx8, 1.5V DDR3 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		-BE	-CG	-BE	-CG	
61	Module thickness (Max)	Back: 1 < thickness ≤ 2 mm, Front: 1 < thickness ≤ 2 mm,		11		
62	Raw Card ID reference	Raw Card F		05		
63	DRAM address mapping edge connector	Undefined		00		
64-116	Reserved			--		
117-118	Module manufacture ID			830B		
119-125	Module information			--		
126-127	CRC			84E6	56C0	
128-145	Module part number	Undefined		--		
146	Module die revision	Undefined		00		
147	Module PCB revision	Nanya Technology		00		
148-149	DRAM device manufacturer ID			830B		
150-175	Manufacturer reserved	Undefined		--		
176-255	Customer reserved			--		

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Environmental Requirements

Symbol	Parameter	Rating	Units
T_{OPR}	Operating Temperature (ambient)	0 to 65	°C
T_{STG}	Storage Temperature	-50 to 100	°C

Note: Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Note
V_{DD}	Voltage on VDD pins relative to Vss	-0.7 to 1.95	V	1, 2
V_{DDQ}	Voltage on VDDQ pins relative to Vss	-0.5 to 1.95	V	1, 3
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.5 to 1.95	V	1
T_{STG}	Storage Temperature	-55 to 95	°C	1, 2

Note:
1. Stresses greater than those listed under "Absolute Maxiumum Ratings" may cause permenent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please referto JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times.

Operating temperature Conditions

Symbol	Parameter	Rating	Units	Note
T_{CASE}	Operating Temperature (Ambient)	0 to 95	°C	1

Note:
1. Case temperature is measured at top and center side of any DRAMs.
2. T_{CASE} > 85°C ➔ t_{REFI} = 3.9 µs

DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V_{DDQ}	Output Supply Voltage	1.425	1.5	1.575	V	1,2

Note:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

Single Ended AC and DC Input Levels

Symbol	Parameter	DDR3-1066, DDR3-1333		Units	Note
		Min.	Max.		
VIH (DC)	DC input logic high	Vref + 0.100	VDD	V	1
VIL (DC)	DC input logic low	VSS	Vref – 0.100	V	1
VIH (AC)	AC input logic high	Vref + 0.175		V	1
VIL (AC)	AC input logic low	-	Vref – 0.175	V	1
VrefDQ(DC)	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	V	2,3
VrefCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	2,3

Note:
1. For DQ and DM, Vref = VrefDQ. For input only pins except $\overline{\text{RESET}}$, Vref = VrefCA.
2. The AC peak noise on Vref may not allow Vref to deviate from Vref(DC) by more than +/- 1% VDD.
3. For reference: approx. VDD/2 +/- 15mV.

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Operating, Standby, and Refresh Currents

T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.5V ± 0.075V (1GB, 2Ranks, base on 64Mx16 DDR3 SDRAMs)

Symbol	Parameter/Condition	DDR3-1066	DDR3-1333	Unit
I_{DD0}	Operating Current: one bank activate/Precharge	554	598	mA
I_{DD1}	Operating Current: one bank activate/Read/Precharge	664	752	mA
$I_{DD2P(0)}$	Precharge Power-Down Current Fast Exit-MR0 bit A12=0	141	141	mA
$I_{DD2P(1)}$	Precharge Power Down Current Slow Exit-MR0 bit A12=1	264	264	mA
I_{DD2N}	Precharge Standby Current	572	616	mA
I_{DD2Q}	Precharge Quiet Standby current	484	528	mA
I_{DD3P}	Active Power-Down Current Always Fast Exit	352	396	mA
I_{DD3N}	Active Standby Current	572	616	mA
I_{DD4W}	Operating Current: Burst Write	1258	1522	mA
I_{DD4R}	Operating Current: Burst Read	1082	1258	mA
I_{DD5B}	Burst Refresh Current	1170	1258	mA
I_{DD6}	Self-Refresh Current Normal Temperature Range (0-85C)	123	123	mA
I_{DD7}	All Bank Interleave Read Current	1522	1830	mA
Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.				

Operating, Standby, and Refresh Currents

T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.5V ± 0.075V (2GB, 2Ranks, base on 128Mx8 DDR3 SDRAMs)

Symbol	Parameter/Condition	DDR3-1066	DDR3-1333	Unit
I_{DD0}	Operating Current: one bank activate/Precharge	1109	1197	mA
I_{DD1}	Operating Current: one bank activate/Read/Precharge	1241	1329	mA
$I_{DD2P(0)}$	Precharge Power-Down Current Fast Exit-MR0 bit A12=0	282	282	mA
$I_{DD2P(1)}$	Precharge Power Down Current Slow Exit-MR0 bit A12=1	528	528	mA
I_{DD2N}	Precharge Standby Current	1144	1232	mA
I_{DD2Q}	Precharge Quiet Standby current	968	1056	mA
I_{DD3P}	Active Power-Down Current Always Fast Exit	704	792	mA
I_{DD3N}	Active Standby Current	1144	1232	mA
I_{DD4W}	Operating Current: Burst Write	1549	1901	mA
I_{DD4R}	Operating Current: Burst Read	1549	1901	mA
I_{DD5B}	Burst Refresh Current	2341	2517	mA
I_{DD6}	Self-Refresh Current Normal Temperature Range (0-85C)	246	246	mA
I_{DD7}	All Bank Interleave Read Current	2781	3309	mA
Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.				

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Speed Bins

Speed Bin			DDR3-1066 (-BE)		DDR3-1333(-CG)		Unit
CL - nRCD - nRP			7-7-7		9-9-9		
Parameter		Symbol	Min	Max	Min	Max	
Internal read command to first data		tAA	13.125	20	13.5	20	ns
ACT to internal read or write delay time		tRCD	13.125	--	13.5	--	ns
PRE command period		tRP	13.125	--	13.5	--	ns
ACT to ACT or REF command period		tRC	50.625	--	49.5	--	ns
ACT to PRE command period		tRAS	37.5	9*tREFI	36	9*tREFI	ns
CL = 5	CWL=5	tCK(AVG)	Reserved		Reserved		ns
	CWL=6, 7, 8	tCK(AVG)	Reserved		Reserved		ns
CL = 6	CWL=5	tCK(AVG)	2.5	3.3	2.5	3.3	ns
	CWL=6	tCK(AVG)	Reserved		Reserved		ns
	CWL=7, 8	tCK(AVG)	Reserved		Reserved		ns
CL = 7	CWL=5	tCK(AVG)	Reserved		Reserved		ns
	CWL=6	tCK(AVG)	1.875	<2.5	Reserved		ns
	CWL=7	tCK(AVG)	Reserved		Reserved		ns
	CWL=8	tCK(AVG)	Reserved		Reserved		ns
CL = 8	CWL=5	tCK(AVG)	Reserved		Reserved		ns
	CWL=6	tCK(AVG)	1.875	<2.5	1.875	<2.5	ns
	CWL=7	tCK(AVG)	--		Reserved		ns
	CWL=8	tCK(AVG)	--		Reserved		ns
CL = 9	CWL=5, 6	tCK(AVG)	--		Reserved		ns
	CWL=7	tCK(AVG)	--		1.5	<1.875	ns
	CWL=8	tCK(AVG)	--		Reserved		ns
CL = 10	CWL=5, 6	tCK(AVG)	--		Reserved		ns
	CWL=7	tCK(AVG)	--		Reserved		ns
	CWL=8	tCK(AVG)	--		1.5 (Optional)	<1.875	ns
CL = 11	CWL=5, 6, 7	tCK(AVG)	--		--		ns
	CWL=8	tCK(AVG)	--		--		ns ns
Supported CL settings			6,7,8		6,8,9,(10)		nCK
Supported CWL Settings			5,6		5,6,7		nCK

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AC Timing Specifications for DDR3 SDRAM Devices Used on Module

		DDR3-1066		DDR3-1333		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**
Clock Timing						
Minimum Clock Cycle time (DLL off mode)	tCK(DLL_OFF)	8	-	8		ns
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg)min +tJIT(per)min	tCK(avg)max +tJIT(per)max	tCK(avg)min +tJIT(per)min	tCK(avg)max +tJIT(per)max	ps
Absolute clock high pulse width	tCH(abs)	0.43	-	0.43	-	ps
Absolute clock low pulse width	tCL(abs)	0.43	-	0.43	-	ps
Clock Period Jitter	tJIT(per)	-90	90	-80	80	ps
Clock Period Jitter during DLL locking period	tJIT(per,lck)	-80	80	-70	70	ps
Cycle to Cycle Period Jitter	tJIT(cc)	180		160		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc,lck)	160		140		ps
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	ps
Cumulative error across 2 cycles	tERR(2per)	-132	132	-118	118	ps
Cumulative error across 3 cycles	tERR(3per)	-157	157	-140	140	ps
Cumulative error across 4 cycles	tERR(4per)	-175	175	-155	155	ps
Cumulative error across 5 cycles	tERR(5per)	-188	188	-168	168	ps
Cumulative error across 6 cycles	tERR(6per)	-200	200	-177	177	ps
Cumulative error across 7 cycles	tERR(7per)	-209	209	-186	186	ps
Cumulative error across 8 cycles	tERR(8per)	-217	217	-193	193	ps
Cumulative error across 9 cycles	tERR(9per)	-224	224	-200	200	ps
Cumulative error across 10 cycles	tERR(10per)	-231	231	-205	205	ps
Cumulative error across n=11~50 cycles	tERR(nper)	tERR(npr)min =(1+0.68ln(n))*tJIT (per)min	tERR(npr)max =(1+0.68ln(n))*tJIT (per)max	tERR(npr)min =(1+0.68ln(n))*tJIT (per)min	tERR(npr)max =(1+0.68ln(n))*tJIT (per)max	ps
Data Timing						
DQS, $\overline{DQS}$ to DQ skew, per group, per access	tDQSQ	-	150		125	ps
DQ output hold time from DQS, $\overline{DQS}$	tQH	0.38	-	0.38		tCK(avg)
DQ low-impedance time from CK, $\overline{CK}$	tLZ(DQ)	-600	300	-500	250	ps
DQ high-impedance time from CK, $\overline{CK}$	tHZ(DQ)	-	300		250	ps
Data setup time to DQS, DQS reference to Vih(ac) / Vil(ac) levels	tDS(base)	25		TBD		ps
Data hold time to DQS, DQS reference to Vih(ac) / Vil(ac) levels	tDH(base)	100		TBD		ps
Data Strobe Timing						
DQS, $\overline{DQS}$ differential READ Preamble	tRPRE	0.9	-	0.9	-	tCK(avg)
DQS, $\overline{DQS}$ differential READ Postamble	tRPST	0.3	-	0.3	-	tCK(avg)
DQS, $\overline{DQS}$ differential output high time	tQSH	0.38	-	0.40		tCK(avg)
DQS, $\overline{DQS}$ differential output low time	tQSL	0.38	-	0.40		tCK(avg)
DQS, $\overline{DQS}$ differential WRITE Preamble	tWPRE	0.9	-	0.9		tCK(avg)
DQS, $\overline{DQS}$ differential WRITE Postamble	tWPST	0.3	-	0.3		tCK(avg)
DQS, $\overline{DQS}$ rising dege output access time from rising CK, $\overline{CK}$	tDQSCK	-300	300	-255	255	ps
DQS, $\overline{DQS}$ low-impedance time (Reference from RL-1)	tLZ(DQS)	-600	300	-500	250	ps
DQS, $\overline{DQS}$ high-impedance time (Reference from RL + BL/2)	tHZ(DQS)	-	300		250	ps
DQS, $\overline{DQS}$ differential input low pulse width	tDQSL	0.4	0.6	0.4	0.6	tCK(avg)
DQS, $\overline{DQS}$ differential input high pulse width	tDQSH	0.4	0.6	0.4	0.6	tCK(avg)
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	tDQSS	-0.25	0.25	-0.25	0.25	tCK(avg)
DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge	tDSS	0.2	-	0.2	-	tCK(avg)
DQS, $\overline{DQS}$ falling edge hold time to CK, $\overline{CK}$ rising edge	tDSH	0.2	-	0.2	-	tCK(avg)

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		DDR3-1066		DDR3-1333		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**
Command and Address Timing						
DLL locking time	tDLLK	512	-	512	-	nCK
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	
WRITE recovery time	tWR	15	-	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	4	-	nCK
Mode Register Set command update delay	tMOD	max(12nCK, 15ns)	-	max(12nCK, 15ns)	-	
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	4	-	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP/tCK(avg))				nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4nCK, 7.5ns)	-	max(4nCK, 6ns)	-	
Four activate window for 1KB page size	tFAW	37.5	-	30	-	ns
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	tIS(base)	125	-	65	-	ps
Command and Address hold time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	tIH(base)	200	-	140	-	ps
Calibrating Timing						
Power-up and RESET calibration time	tZQinit	512	-	512	-	nCK
Normal operation Full calibration time	tZQoper	256	-	256	-	nCK
Normal operation Short calibration time	tZQCS	64	-	64	-	nCK
Reset Timing						
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	
Self Refresh Timings						
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	nCK
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKE(min) + 1nCK	-	tCKE(min) + 1nCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	
Valid Clock Requirement after Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	
Power Down Timings						
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nCK, 7.5ns)	-	max(3nCK, 6ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10nCK, 24ns)	-	max(10nCK, 24ns)	-	
CKE minimum pulse width	tCKE	max(3nCK, 5.625ns)	-	max(3nCK, 5.625ns)	-	
Command pass disable delay	tCPDED	1	-	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL+2+WR+1	-	WL+2+WR+1	-	nCK
Timing of REF command to Power down entry	tREFPDEN	1	-	1	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	

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		DDR3-1066		DDR3-1333		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**
ODT Timings						
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	6	-	nCK
Asynchronous RTT turn-on delay (Power - Down with DLL frozen)	tAONPD	1	9	1	9	ns
Asynchronous RTT turn-off delay (Power – Down with DLL frozen)	tAOFPD	1	9	1	9	ns
RTT turn-on	tAON	-300	300	-250	250	ps
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	tCK(avg)
Write Leveling Timings						
First DQS/$\overline{DQS}$ rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	nCK
DQS/DQS delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	nCK
Write leveling setup time from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing	tWLS	245	-	195	-	ps
Write leveling setup hold from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing	tWLH	245	-	195	-	ps
Write leveling output delay	tWLO	0	9	0	9	ns
Write leveling output error	tWLOE	0	2	0	2	ns

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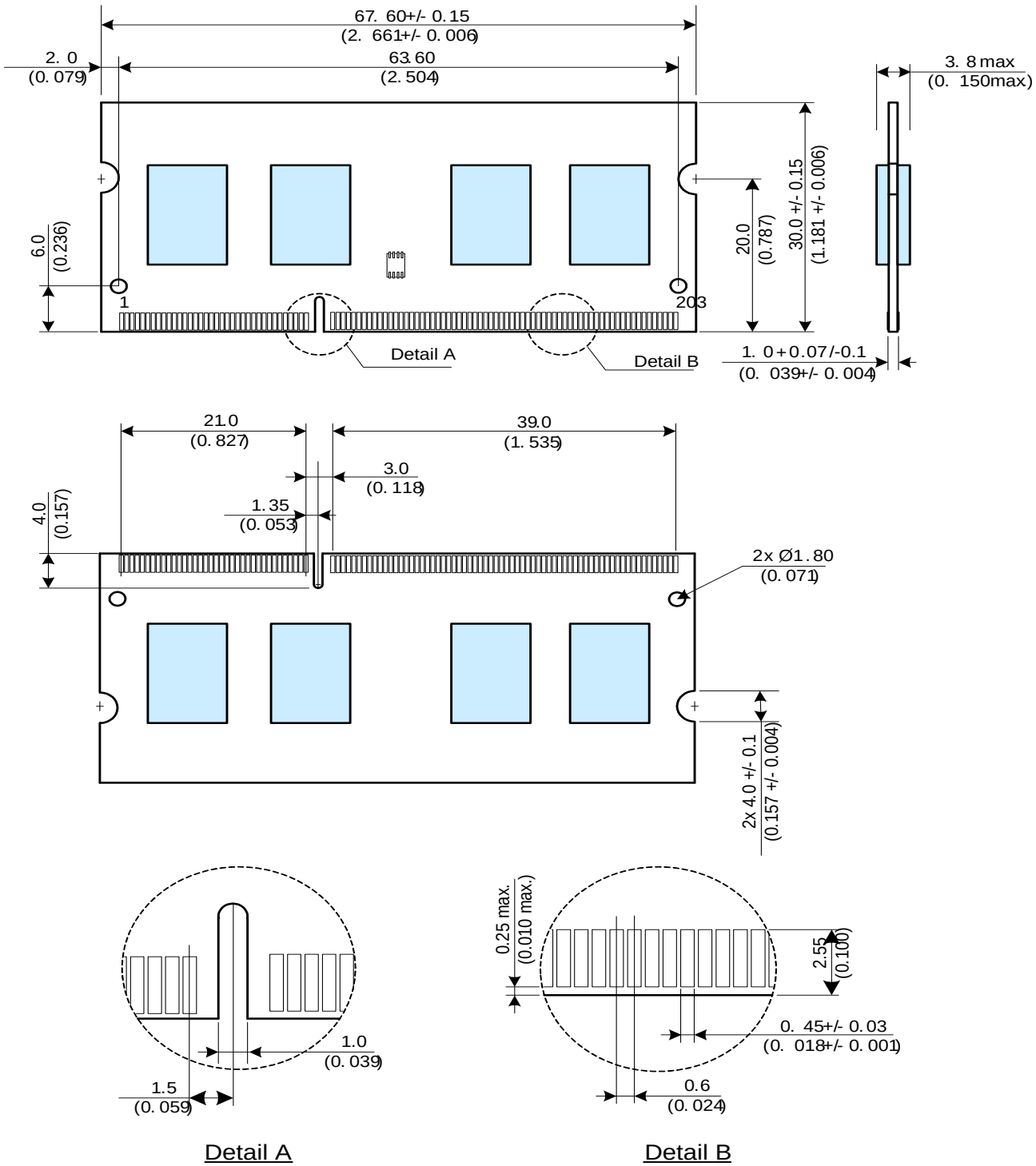
Package Dimensions

[1GB – 2 Ranks, 64Mx16 DDR3 SDRAMs]



Detail A

Detail B

Units: Millimeters(Inches)

Note: Device position and scale are only for reference.

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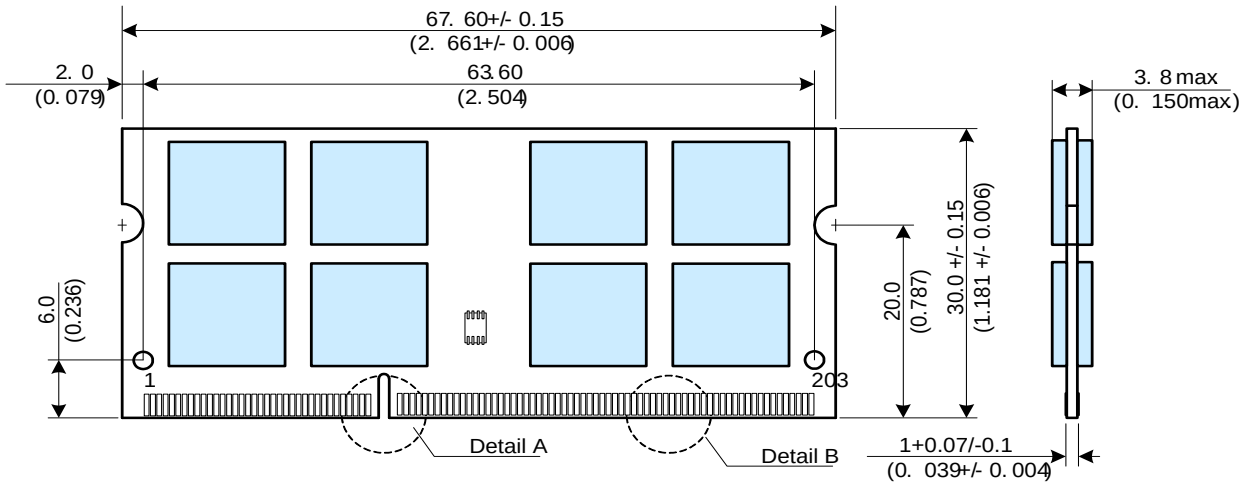
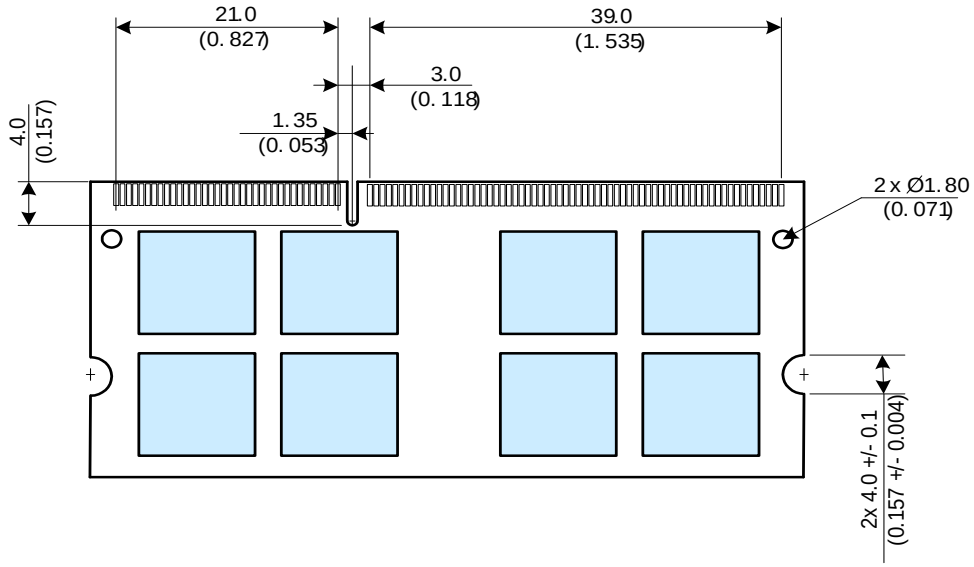
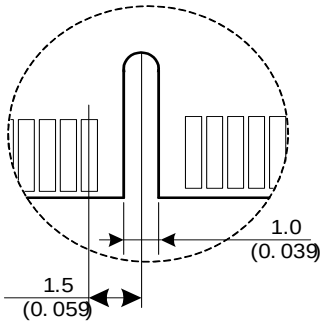
Package Dimensions

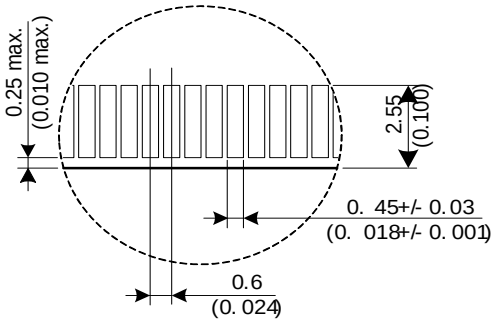
[2GB – 2 Ranks, 128Mx8 DDR3 SDRAMs]







Detail A



Detail B

Units: Millimeters(Inches)

Note: Device position and scale are only for reference.

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Revision Log

Rev	Date	Modification
0.1	07/2008	Preliminary edition
1.0	09/2008	Official Release
1.1	04/2009	Re-move A4P, A4N Part Numbers; Add A5P and A5N Part Numbers.

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